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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/448,884	11/24/1999	JOELLE SHARP	18865-003600	5563

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EXAMINER

VU, DAVID

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/448,884

Applicant(s)

SHARP ET AL.

Examiner

DAVID VU

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 15-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 and 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim et al.,(US 6,228,727).

Lim et al, in related text and figures (Figs. 7-12) disclose a method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and by a closed end within the body of the substrate, the method comprising the steps of:

- (a) providing a substrate;
- (b) growing a masking layer on the major surface of the substrate;
- c) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access;

(d) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench; (Col. 2, Lines. 30-32)

(e) removing the selectively etched masking layer; and

(f) annealing the trench in hydrogen ambient with a temperature of between about 800-1200°C to reduce the number of defects in the trench created during the step of forming, and to round corners at the open and closed ends of the trench (Col. 4, Lines. 38-47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al., (US 5,943,581) in view of Lim et al. (US 6,228,727).

Lu et al., in related text, (Col. 4, Lines. 39-44; Col. 5, Lines. 37-41) and figures (Fig. 1-8) disclose a method of making a trench field effect transistor, comprising:

(a) providing a semiconductor substrate 10 of an N dopant charge type, the substrate embodying the drain of the trench field effect transistor (Col. 6, Lines. 19-32 and Fig. 8);

(b) growing an epitaxial layer 14 of the same N+ dopant charge type on the substrate 10, the epitaxial layer having a different resistivity than the resistivity of the substrate;

(c) growing a masking layer 22 on the major surface of the substrate 10 (Col. 6, Lines. 48-56);

(d) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access; (Col. 6, Lines. 56-59)

(e) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench; (Col. 7, Lines. 5-15)

(f) removing the selectively etched masking layer 22 (Col. 7, Lines. 28-30); and

(g) forming at least one trench into the epitaxial layer, each trench defined by a first end in a plane defined by a major surface of the substrate and by walls that extend to a second end at a predetermined depth into the epitaxial layer 14;

(h) growing a dielectric layer 26 on the walls of the at least one trench; (Col. 7, Lines. 30-44 and Fig. 7)

(i) forming a conductor 28 over the dielectric layer 26, the conductor embodying the gate of the trench field effect transistor; (Col. 7, Lines. 45-67 and Fig. 7)

(j) patterning the epitaxial layer and implanting a dopant of a second charge type to form p-wells interposed between adjacent trenches; (Fig. 7) and

(k) patterning the epitaxial layer and implanting a dopant of the n-type to form regions that embody the source regions of the field effect transistor. (Fig. 8)

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the exposed sidewall surfaces of trench are annealed in a hydrogen ambient environment. Lim et al., in related text, (Col. 4, Lines. 38-47) disclose the step of annealing the sidewall surfaces of trench using hydrogen gas at the temperatures of between about 800-1200°C. However, given the

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substantial Lu et al., in view of Lim et al., it would have been obvious to one with ordinary skill in the art at the time of the invention for annealing the trench to reduce the number of defects in the trench created during the step of forming, and to round corners at the open and closed ends of the trench.

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the annealing pressure. However, given the substantial Lu et al., in view of Lim et al., it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the optimum the annealing temperature and pressure through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

In re claim 20, Lu et al., in related text disclose further including the step of forming one or more heavy bodies of the second charge type positioned above the wells and between the source regions, each heavy body forming an abrupt junction with its corresponding well. (Col. 8, Lines. 33-67).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

David Vu
DV


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PRIMARY EXAMINER